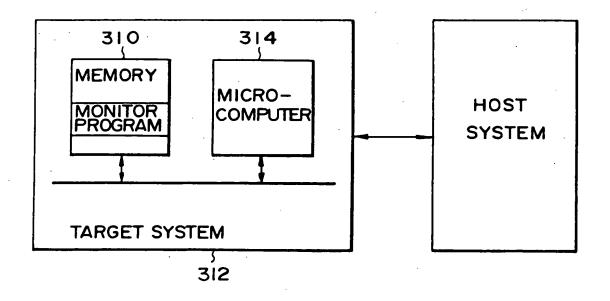
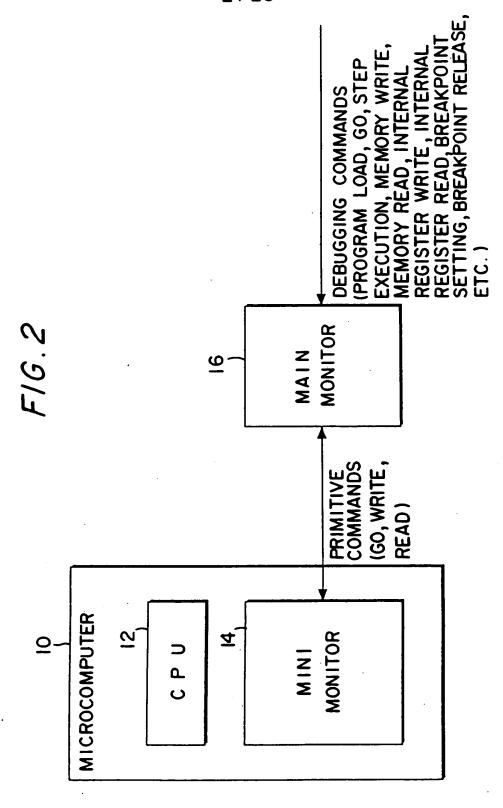


FIG. 1B





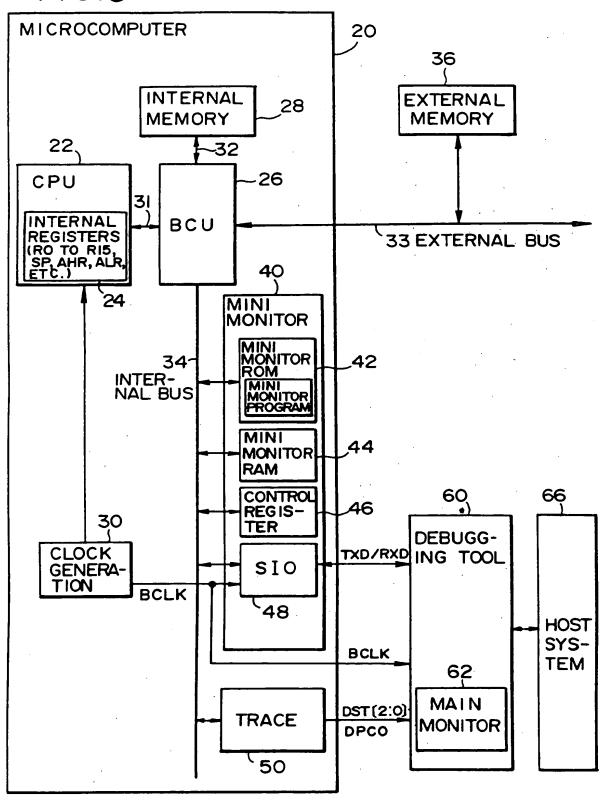


FIG. 4

#### MEMORY MAP IN DEBUGGING MODE

		IOOL
FFFFFF		]
	EXTERNAL MEMORY	·
1 1 1 1	EXTERNAL I/O	
1 1 1	EXTERNAL MEMORY	
,   	EXTERNAL MEMORY	
; ! !	INTERNAL ROM	
1 1 1 1	CONTROL REGISTER (STEP EXECUTION ENABLE BIT, BREAK ENABLE BIT, BREAK ADDRESS BIT, ETC.)	✓ DI
<b>!</b> .	MINI MONITOR RAM	D2
1	MINI MONITOR ROM	D3
1	INTERNAL PERIPHERAL CIRCUITRY	
0000000h	INTERNAL RAM	

# FIG. 54

PROGRAM LOAD

$$\left( \begin{array}{c} \text{80010h, I2 BYTES, ADD ---, SUB ---} \\ \text{AND ---, OR ---, XOR ---, LD.W ---} \\ \end{array} \right) \longrightarrow + \text{WRITE (80014h, ADD ---, OR ---)} \\ + \text{WRITE (80018h, XOR ---, LD.W ---)}$$

STEP EXECUTION

F16.5C

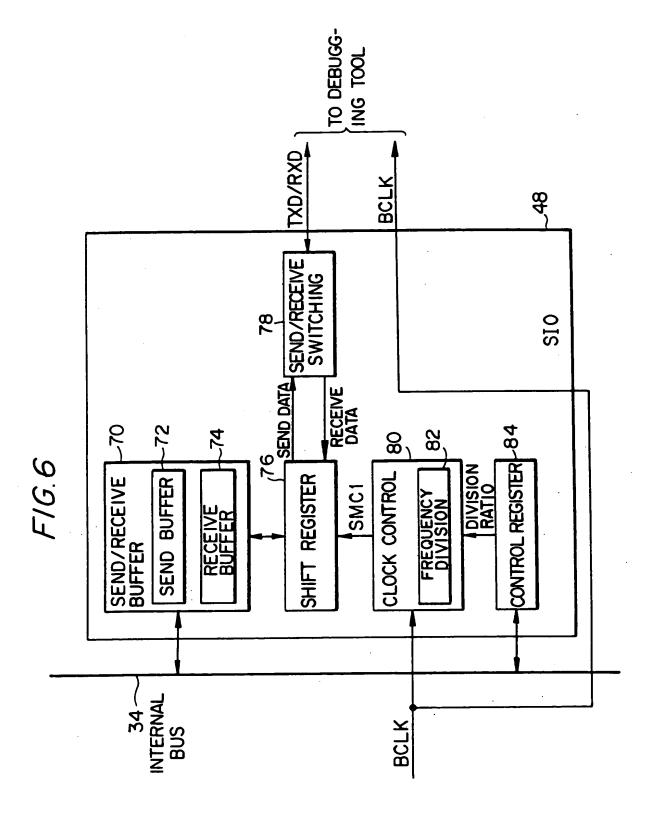
WRITE TO STEP EXECUTION ENABLE CONTROL REGISTER

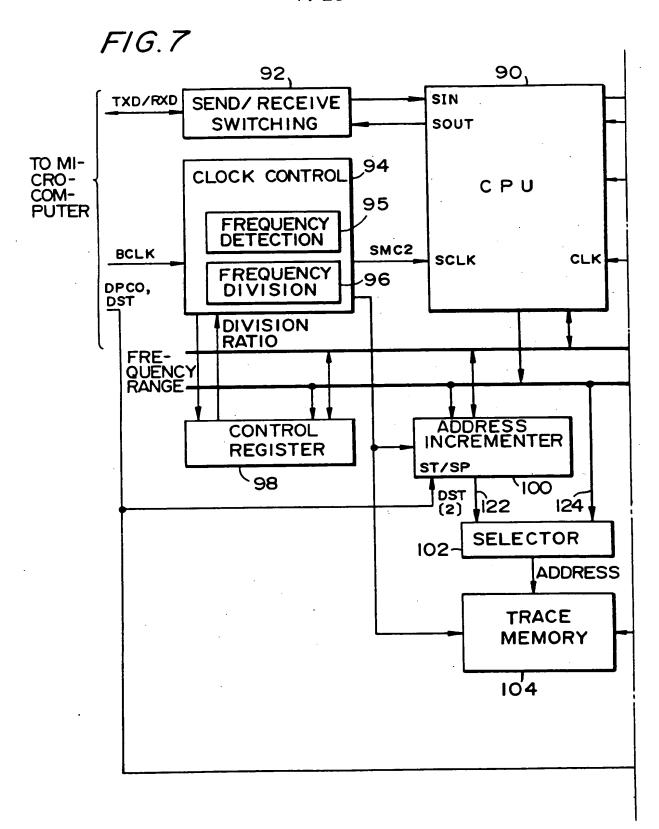
9+

READ MONITOR RAM ON MEMORY MAP INTERNAL REGISTER READ -

FIG.50 BREAKPOINT SETTING

WRITE TO BREAK ENABLE BIT AND BREAK ADDRESS BIT OF CONTROL REGISTER





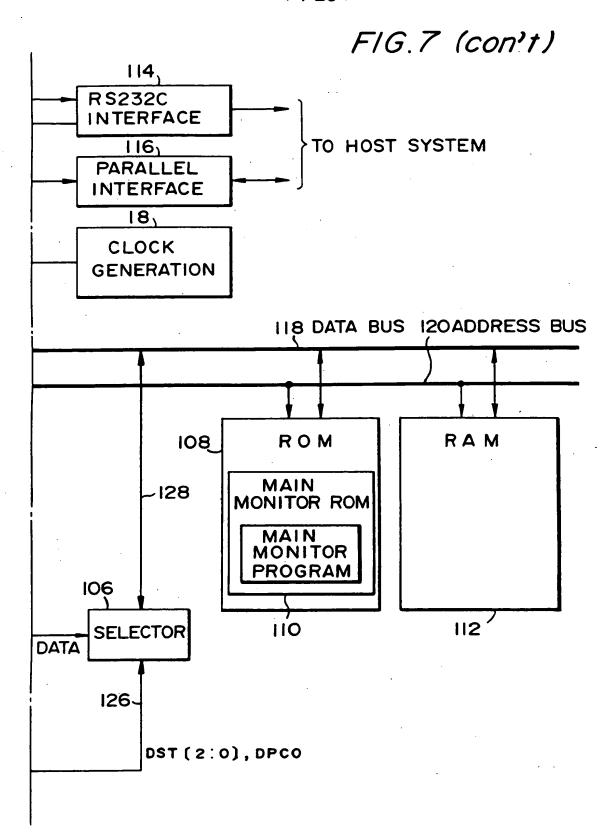


FIG.8A

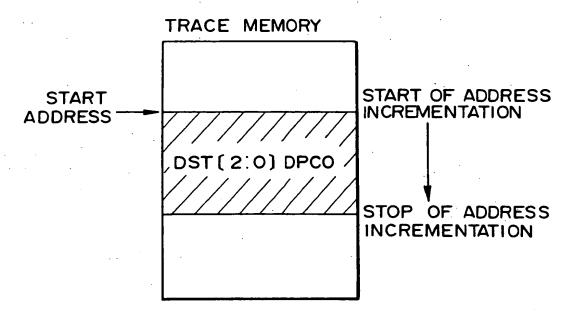


FIG.8B

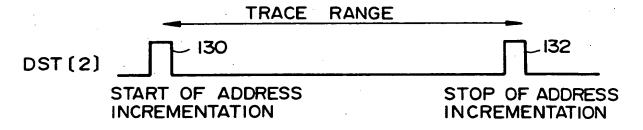
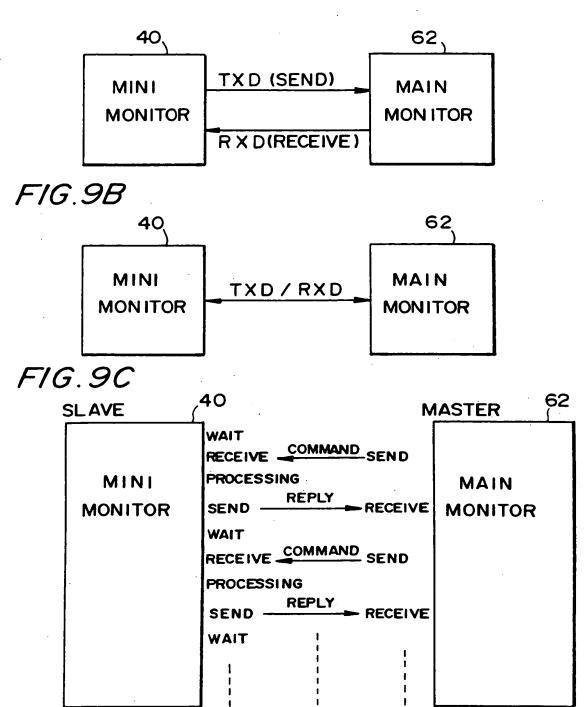


FIG. 9A



# FIG. IOA DATA FORMAT

	•
I D DATA SIZE ADDRESS DATA 1 DATA 2	I BYTE I BYTE 4 BYTES 4 BYTES 4 BYTES 4 BYTES
F1G. 10B GO CO	DMMAND
RECEIVE DATA OOh	NO SEND DATA. SHIFT TO EXECUTION
FIG. 10C WRITE	COMMAND
OIH  WRITE ADDRESS WRITE DATA 1 WRITE DATA 2	——————————————————————————————————————
	COMMAND
RECEIVE DATA O2h  READ ADDRESS	SEND DATA  SEND DATA  READ DATA 1  READ DATA 2

# FIG. I IA

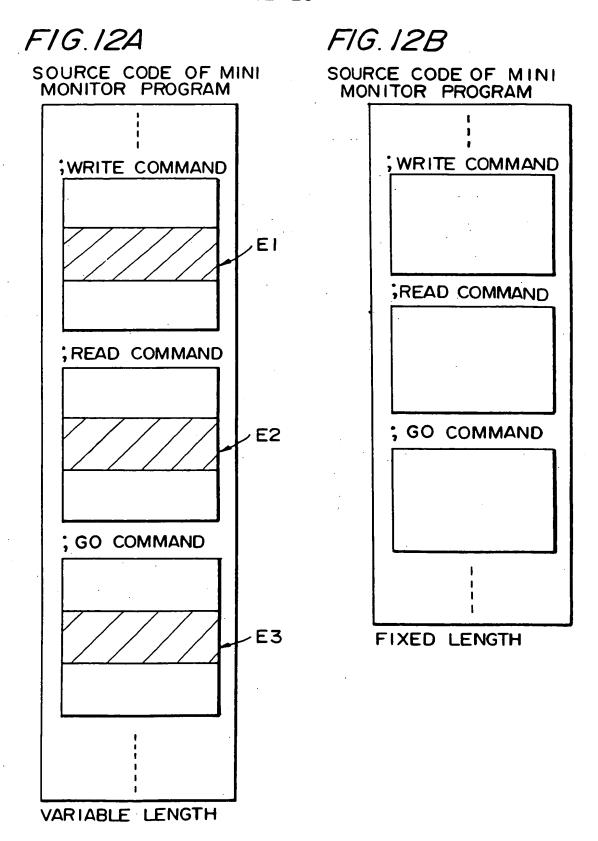
#### EXTERNAL ROUTINE JUMP COMMAND

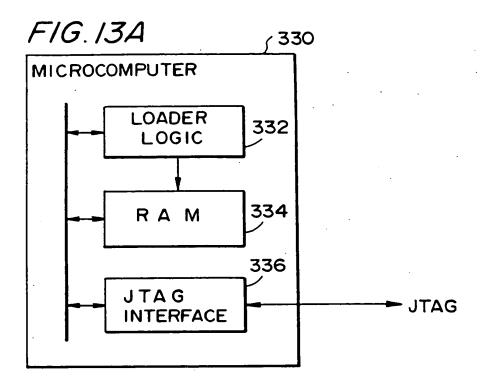
F	RECEIVE DA	TA S	SEND DATA	
	03h			
	18h	(DATA FOR CHECK- ING MALFUNCTION)		
	%R12	(ROUTINE ADDRESS)		, 
	%RI3	(WRITE DATA)	% R10	(RETURN VALUE. WHEN IT IS ZERO, PROGRAM NORMALLY
	%RI4	(DATA ADDRESS)	· <del></del>	TERMINATES)

FIG. I IB

DATA FILL COMMAND

RECEIVE DAT	Δ :	SEND DATA
04 h	·	
1,2,4		
START ADDRESS		
FILL NUMBER		04h
FILL PATTERN		





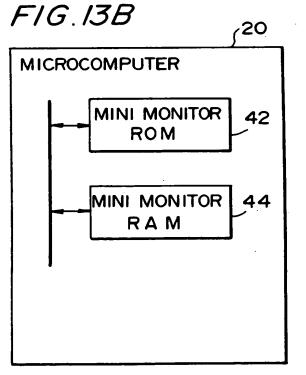
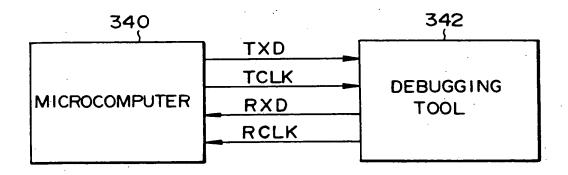
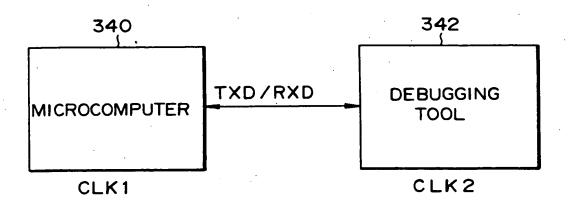


FIG. 14A



F1G.14B



F16.154

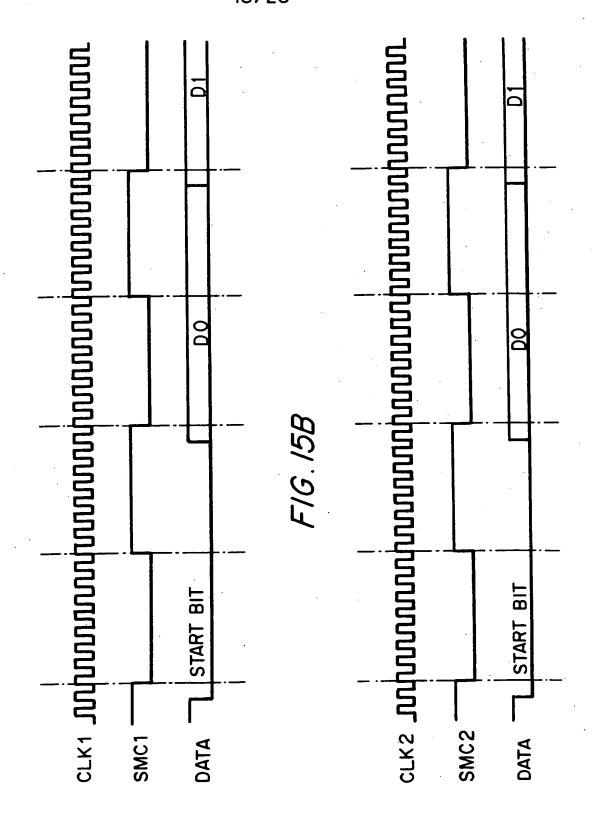
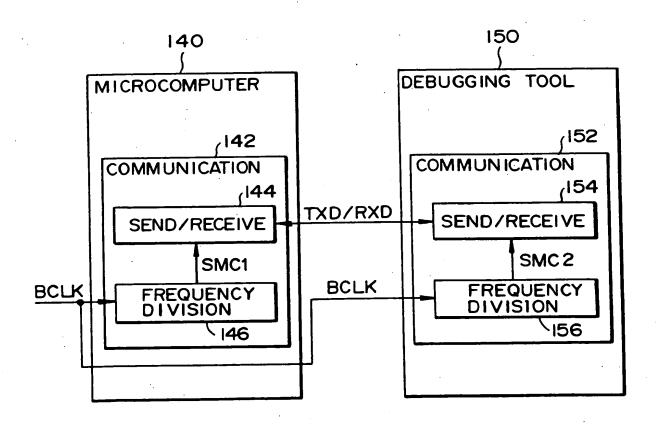
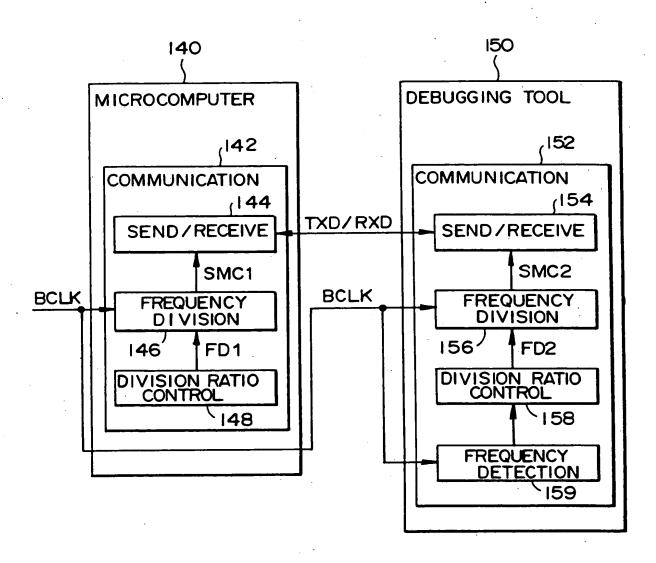


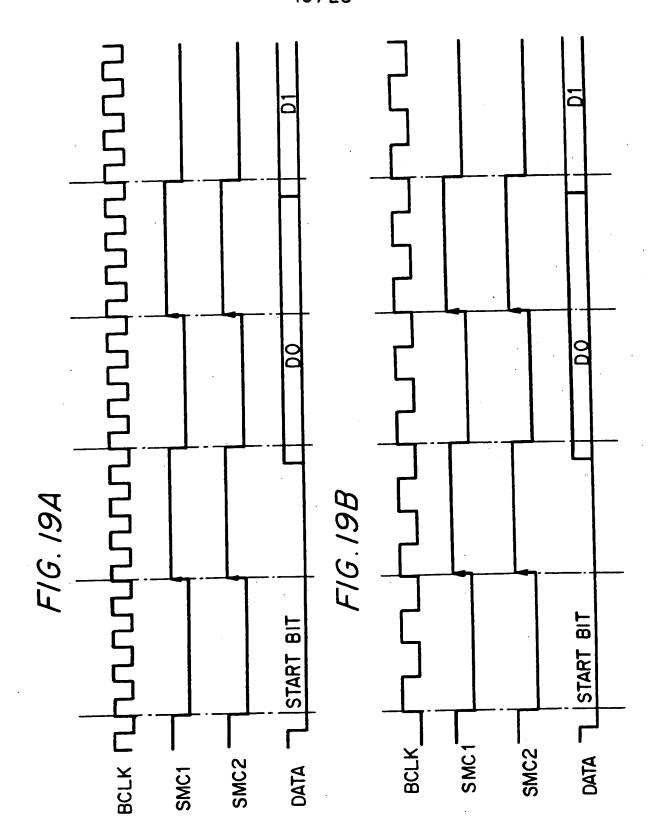
FIG. 16



F16.17B F16.17A START BIT START BIT SMC2 DATA SMC1 DATA

FIG. 18





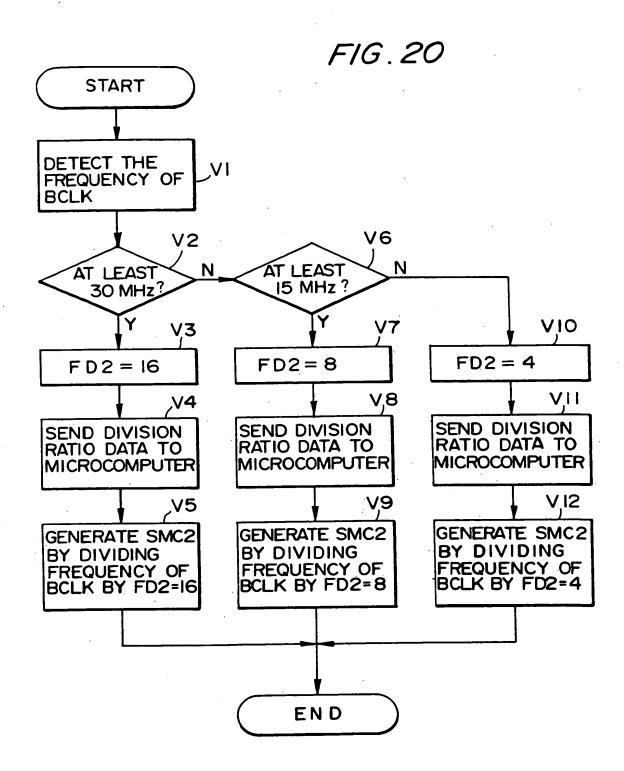


FIG. 21

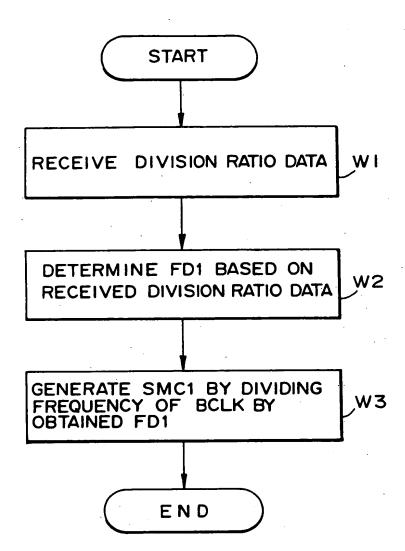


FIG .22

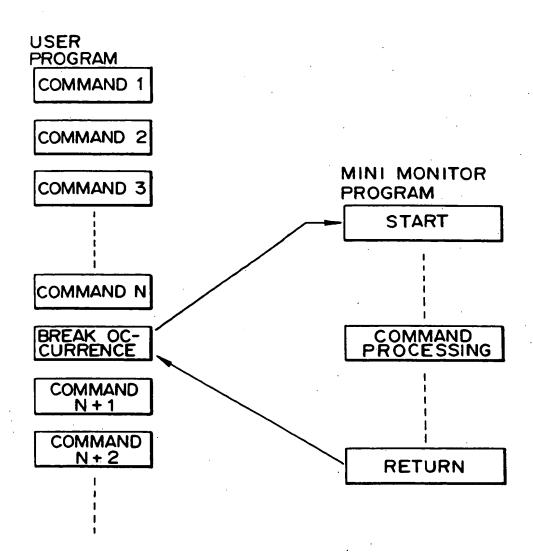


FIG.23

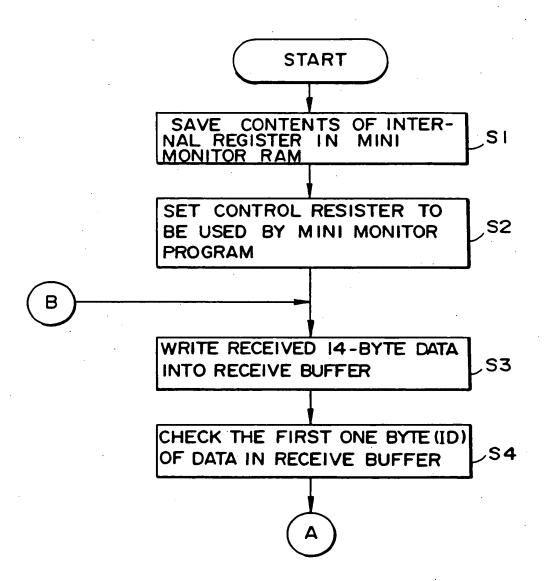
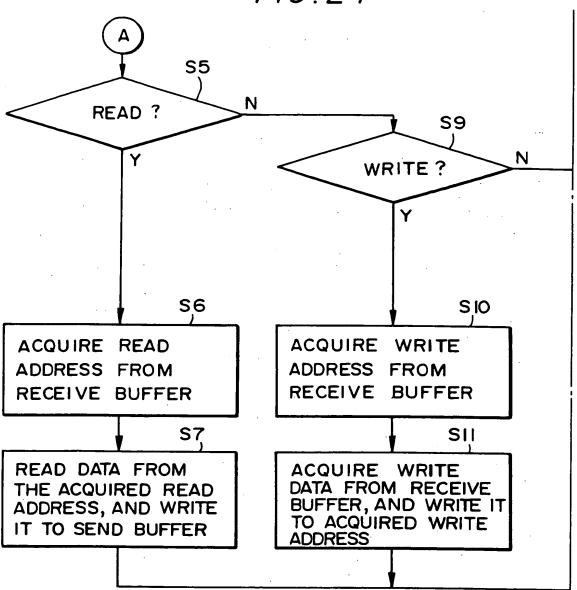
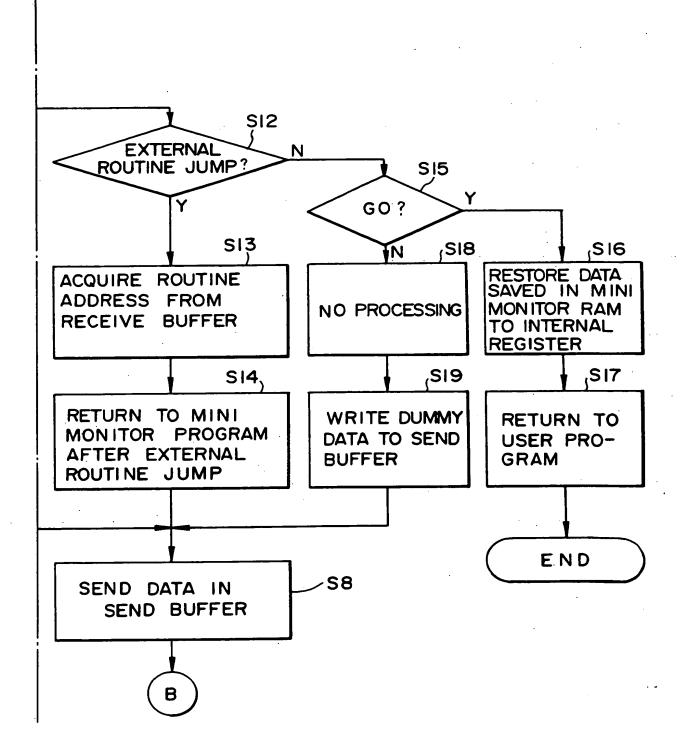
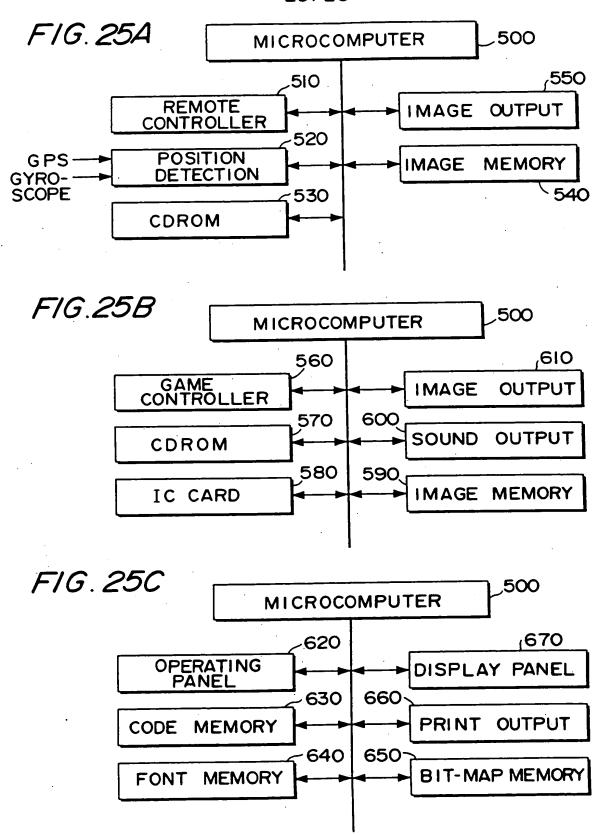


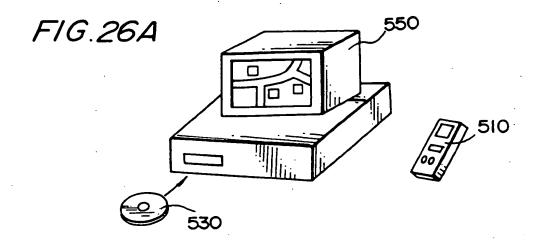
FIG. 24



### FIG.24 (con't)







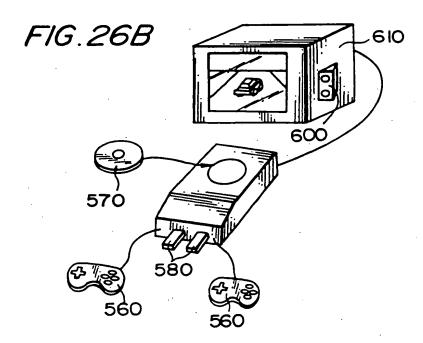


FIG.26C

